Efficient Solution Method for Unified Nonlinear Microwave Circuit and Numerical Solid-State Device Simulation

Gregory B. Tait, *Member, IEEE*

Abstract—**A simple and very efficient harmonic-balance technique is presented that is suitable for the steady-state analysis of nonlinear microwave and millimeter-wave circuits that require physics-based, fully numerical simulations of charge carrier transport in the solid-state device. The practical integration of a numerical device simulator with a nonlinear circuit simulator requires a robust and fast circuit solution algorithm. The new circuit solution algorithm was applied to a test simulation of a 100- to 300-GHz multiplier circuit, achieving a savings in computational effort of 98% and a reduction in execution time by a factor of 33 over contending harmonic-balance techniques.**

I. Introduction

IN MODERN computer-aided analyses of microwave, millimeter-wave, and submillimeter-wave circuits, harmonic-balance techniques are generally employed to characterize the interaction between nonlinear active devices and their linear embedding circuits. Typically, active devices are modeled by lumped quasi-static equivalent circuits or closed-form analytical expressions governing terminal quantities. Such models, however, have limited validity at high frequencies and require significant insight into device operation in order to develop an equivalent circuit topology. Furthermore, the process of assigning values to the elements of the equivalent circuit as functions of bias, frequency, and temperature is a laborious and often non-unique task, requiring extensive experimental or simulated data. An alternative approach is to utilize a physics-based numerical device simulator. Given the importance of both the nonlinear device and its embedding circuit in the design of high-frequency circuits, a full time-dependent device simulator can be combined with harmonic-balance circuit analysis to provide a truly integrated computer-aided design environment. Complete microwave circuits can, therefore, be co-designed from both a device and circuit point of view by specifying device physical properties and circuit embedding impedances. Compared to quasi-static equivalent circuits, hydrodynamic and particle-based device simulators more accurately describe the dynamic high-frequency nonstationary behavior of charge carriers in large-signal devices, yielding better agreement between simulated results and actual measured circuit performance.

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The author is with the Department of Electrical Engineering and Computer Science, United States Military Academy, West Point, NY 10996 USA.
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Despite advances in high-speed computer workstations, the direct incorporation of a physics-based numerical device simulator into a nonlinear circuit simulator continues to strain computational resources. Currently, the implementation of physical device models in circuit analysis is feasible only through intermediate "behavioral" models, such as equivalent circuits or analytical expressions, constructed prior to the actual circuit simulation [1], [2].

In this letter, a simple and efficient method for the analysis of nonlinear microwave circuits is demonstrated. This method, designated the accelerated fixed-point (AFP) algorithm, is motivated by the widely-used multiple reflection (MR) algorithm [3] and is particularly suited for circuit analyses that require full numerical simulations of the high-frequency solid-state devices. The AFP algorithm exhibits enhanced performance over the MR algorithm and other contending harmonic-balance techniques.

II. Accelerated Fixed-Point Iterative Solution Method

Three widely-used numerical solution techniques for harmonic-balance analyses of nonlinear circuits are based on Newton's method, optimization, and the multiple-reflection (MR) algorithm [3]–[5]. For circuit analyses where the nonlinear device will be described by a fully numerical device simulator, the solution method of choice would appear to be the MR algorithm. This approach avoids the repetitive derivative calculations that characterize the Newton and optimization methods. Indeed, generating derivatives from a purely numerical, "black-box" description of the nonlinear device is not practical. Another important advantage of the MR algorithm is that it does not require an initial estimate of the solution, making it attractive for use in general purpose computer programs.

The origin of the robust convergence properties of the MR algorithm can be traced to its use of incident and reflected harmonic voltage waves as the state variables, since this takes advantage of the subunitary nature of scattering matrices. These waves, propagating over a fictitious lossless transmission line inserted between the linear and nonlinear subcircuits, are composed of linear combinations of the total harmonic voltages and currents at the terminals of the nonlinear subcircuit. Unfortunately, the time-domain analysis of the nonlinear subcircuit requires that the voltage wave incident on it (multiplied by a factor of two) be sourced through an impedance equal to the characteristic impedance Z_0 of the fictitious transmission line. In this manner, the total voltage across the device terminals, necessary for device simulation, can be obtained. Hence, the nonlinear subcircuit would have to be solved using an explicit time-discretization finite-difference scheme. Very small time steps Δt would be necessary to maintain reasonable accuracy and avoid numerical instabilities. Numerical device simulators employing implicit time-discretization schemes allow much larger time steps. Therefore, the MR algorithm cannot utilize the efficiency of modern device simulators. The problem is exacerbated whenever it is necessary to simulate several oscillation periods to achieve at least one "clean" steady-state cycle for Fourier analysis. When a device equivalent circuit or analytical model is utilized, it should also be noted that the time integration of the nonlinear circuit differential equations can be a primary source of instability, and high-order, step-controlled Runge-Kutta methods are typically needed. Here too, Runge-Kutta methods are computationally expensive, requiring numerous function evaluations for every time step taken. In any case, it is desirable to have available an algorithm that inherits the good convergence properties of the MR algorithm, but impresses the total time-dependent voltage $v(t)$ directly across the terminals of the nonlinear device. This would maximize the efficiency of numerical simulators. For equivalent circuits, appropriate partitioning of intrinsic device elements to the linear and nonlinear subcircuits (as can be done for diodes and FET's) would eliminate the time-integration process altogether, since the analytically known voltage waveform $v(t)$ would now appear directly across the terminals of the nonlinear elements.

An algorithm that meets these objectives was devised by performing the following steps:

1) The MR algorithm is formulated as a fixed-point iterative scheme, yielding a new voltage component $V_{n,k+1}$ at the device for harmonic number n and iteration step $k+1$ as a nonlinear mapping of $V_{n,k}$:

$$V_{n,k+1} = \frac{2Z_0}{Z_n^L + Z_0} \frac{Z_{n,k}^{\mathrm{NL}}}{Z_{n,k}^{\mathrm{NL}} + Z_0} V_n^S + \frac{Z_n^L - Z_0}{Z_n^L + Z_0} \frac{Z_{n,k}^{\mathrm{NL}}}{Z_{n,k}^{\mathrm{NL}} + Z_0} (V_{n,k} - I_{n,k}Z_0) \tag{1}$$

where, $Z_{n,k}^{\mathrm{NL}} = \frac{V_{n,k}}{I_{n,k}}$ is the nonlinear device impedance for harmonic number n and iteration step k and Z_0, Z_n^L, V_n^S, and $I_{n,k}$ are, respectively, the fictitious transmission line characteristic impedance, the Thevenin equivalent impedance and source voltage of the linear embedding subcircuit at harmonic number n, and the device current component for harmonic number n and iteration step k.

2) For undriven harmonics, $V_n^S = 0$, and the steady-state solution ($k \to \infty$) is known *a priori* from Kirchhoff's voltage law (KVL),

$$Z_n^{\mathrm{NL}} = -Z_n^L \tag{2}$$

TABLE I
THEVENIN EQUIVALENT IMPEDANCES OF THE LINEAR EMBEDDING SUBCIRCUIT AT HARMONIC NUMBER n

n	Z_n^L (Ω)	n	Z_n^L (Ω)
1	12 + j 56	8	0.1 + j 0
2	0 + j 377	9	0.1 + j 0
3	12 + j 20	10	0 1 + j 0
4	0 + j 377	11	0.1 + j 0
5	0 + j 377	12	0 1 + j 0
6	0 + j 377	13	0.1 + j 0
7	0 + j 377		

and is used in (1) to obtain

$$V_{n,k+1} = \frac{Z_n^L}{Z_n^L + Z_0} (V_{n,k} - I_{n,k}Z_0). \tag{3}$$

3) For driven harmonics, a source term containing V_n^S is incorporated in (3) in such a way as to preserve KVL in the eventual steady-state,

$$V_{n,k+1} = \frac{Z_0}{Z_n^L + Z_0} V_n^S + \frac{Z_n^L}{Z_n^L + Z_0} (V_{n,k} - I_{n,k}Z_0) \tag{4}$$

Note that at convergence to the steady state ($k \to \infty$), $V_{n,k+1} = V_{n,k}$ and KVL is satisfied,

$$V_n = V_n^S - I_n Z_n^L \tag{5}$$

Equation (4) can be rewritten as

$$V_{n,k+1} = d_n(V_n^S - I_{n,k} Z_n^L) + (1 - d_n)V_{n,k} \tag{6}$$

where $d_n = \frac{Z_0}{Z_n^L + Z_0}$. Equation (6) is similar to the voltage update method of [6] with the exception that complex under-relaxation parameters d_n are employed that are automatically calculated for each harmonic component of the voltage waveform. These under-relaxation parameters, motivated by the MR algorithm, provide varying degrees of damping for the voltage updates based on the relative magnitudes of the linear embedding impedances Z_n^L. With this automatic scaling of the damping factors, the nonlinear mapping described in (6) is capable of efficiently producing a contracting (Cauchy) sequence with monotonic convergence properties.

4) A Steffensen acceleration scheme for iterative processes is adopted from the secant methods of numerical analysis [7],

$$V_{n,k+1} = \tilde{V}_{n,k+2} + \frac{(\tilde{V}_{n,k+2} - \tilde{V}_{n,k+1})(\tilde{V}_{n,k+2} - \tilde{V}_{n,k+1})}{(\tilde{V}_{n,k+1} - V_{n,k}) - (\tilde{V}_{n,k+2} - \tilde{V}_{n,k+1})} \tag{7}$$

TABLE II
COMPARISON OF THE ACCELERATED FIXED-POINT (AFP) AND MULTIPLE-REJECTION (MR) ALGORITHMS

Algorithm	Z_0 (Ω)	Iterations (k)	Function Evaluations	Relative CPU Time	Power Absorbed (mW)	Power Delivered (mW)
AFP	17.5	21	4,242	1	27.6	1.22
MR	320	265	294,676	33	27.6	1.22

where $\tilde{V}_{n,k+2}$ and $\tilde{V}_{n,k+1}$ are intermediate values calculated from two successive applications of (6), starting with $\tilde{V}_{n,k} = V_{n,k}$. The process in (7) exhibits a superlinear convergence rate, approaching the quadratic rate of Newton's method while not requiring any explicit derivative calculations in any of the steps. Equations (6) and (7) constitute the accelerated fixed-point (AFP) algorithm.

III. RESULTS AND DISCUSSION

To test the new algorithm's performance, a real example of a 100- to 300-GHz frequency multiplier circuit employing a novel heterostructure-barrier varactor (HBV) was chosen [8]. This test case was a difficult one, as the device exhibited significant response in both its nonlinear current-voltage (I-V) and capacitance-voltage (C-V) characteristics, and, furthermore, was pumped at a high input power level. The HBV device model utilized curve fits to the actual measured device I-V and C-V characteristics, shown in [8]. The device series resistance was set at 10 Ω. In the harmonic-balance analysis, 13 harmonics were retained as this number was required to accurately reproduce the device capacitance and conductance time-domain waveforms. Operating conditions consisted of an input signal at 100 GHz with an available power of 30 mW and zero DC-bias voltage. The embedding impedances of the linear subcircuit, as seen by the HBV device, are given in Table I. The impedances at the first and third harmonics have been adjusted to give near-optimum performance. The impedances of the idler (second harmonic) and higher harmonics have been artificially set to provide both "open" and "short" circuits, purposely to stress the convergence performance of the algorithm.

When applied to this problem, the voltage update algorithm of [6] diverged for all values of its adjustable convergence parameter. Both AFP and MR algorithms also have one adjustable convergence parameter, namely Z_0, which was optimized in each algorithm for this problem. The chosen value of Z_0 in both algorithms can have significant impact on their convergence properties. The same discrete Fourier transform subroutine was employed in both codes and utilized 101 time samples per period. Convergence was obtained when the ratios $|(V_n - V_n^S)/I_n|/|Z_n^L|$ were within 0.5% of unity for all n. A useful figure-of-merit for the performance of the algorithms is the function evaluation number, which counts the times that the instantaneous device current is calculated in the time domain from the analytical curve-fit expressions for the HBV device.

Table II clearly shows the significant improvement in efficiency of the AFP algorithm over the MR algorithm, with both methods yielding identical results for the frequency tripler circuit performance. A reduction in computational effort of over 98% is realized in terms of number of function evaluations, and the execution time is reduced by a factor of 33. A comparison of the two algorithms employing a full numerical simulator for the HBV device has not been attempted, due to prohibitively long execution times anticipated for the MR algorithm. However, an integrated HBV hydrodynamic device and harmonic-balance circuit simulator utilizing the AFP algorithm has successfully produced accurate and efficient simulations of HBV frequency tripler circuits in under two hours, providing new information for the co-design of both device and circuit [9]. Finally, the AFP algorithm is easily applied to a variety of high-frequency circuits, such as harmonic transferred-electron oscillators and multiple-barrier semiconductor heterostructure device mixers, detectors, and frequency multipliers [9]–[11].

REFERENCES

[1] F. Filicori, G. Ghione and C. U. Naldi, "Physics-based electron device modeling and computer-aided MMIC design," *IEEE Trans. Microwave Theory Tech.*, vol. 40, no. 7, pp. 1333–1352, July 1992.
[2] J. W Bandler, R. M. Biernacki, and Q. Cai *et al.*, "Integrated physics-oriented statistical modeling, simulation and optimization," *IEEE Trans. Microwave Theory Tech.*, vol. 40, no. 7, pp. 1374–1400, July 1992.
[3] P. H. Siegel, A. R. Kerr, and W. Hwang, "Topics in the optimization of millimeter-wave mixers," NASA Tech. Paper no. 2287, Mar. 1984.
[4] V Rizzoli and A. Neri, "State of the art and present trends in nonlinear microwave CAD techniques," *IEEE Trans. Microwave Theory Tech.*, vol. 36, no. 2, pp. 343–365, Feb. 1988.
[5] S. A. Maas, *Nonlinear Microwave Circuits*. Norwood, MA: Artech House, Inc., 1988.
[6] R. G. Hicks and P. J. Khan, "Numerical analysis of nonlinear solid-state device excitation in microwave circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, no. 3, pp. 251–259, Mar. 1982.
[7] J. Ortega and W. Rheinboldt, *Iterative Solution of Nonlinear Equations in Several Variables*. New York, NY: Academic Press, Inc., 1970.
[8] D. Choudhury, M. A. Frerking, and P. D. Batelaan, "A 200 GHz tripler using a single barrier varactor," *IEEE Trans. Microwave Theory Tech.*, vol. 41, no. 4, pp. 595–599, Apr. 1993.
[9] J. R. Jones, S. H. Jones, and G. B. Tait, "GaAs/InGaAs/AlGaAs heterostructure barrier varactors for frequency tripling," in *Proc. Fifth Int. Symp. on Space Terahertz Technology*, May 1994, Ann Arbor, MI, pp. 497–513.
[10] M. F. Zybura, J. R. Jones, S. H. Jones, and G B. Tait, "Simulation of 100–300 GHz solid-state harmonic sources," to appear in *IEEE Trans. Microwave Theory Tech.*, Apr. 1995.
[11] G. B. Tait, "Microwave mixers employing multiple-barrier semiconductor heterostructure devices," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 9, pp. 1596–1601, Sept. 1994